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Term: 12 with 13

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<u>DB Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	12 with 13	17	<u>L8</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	14 not 16	8	<u>L7</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	12 and 14	10	<u>L6</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	12 same 14	0	<u>L5</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	13 with 11	18	<u>L4</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	configuration adj (logic or memory)	4262	<u>L3</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	system bus	24202	<u>L2</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	dma or dmac or (direct memory access\$3)	27964	<u>L1</u>

<u>DB Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l17 not l18	37	<u>L19</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	(digital signal processor) same l1	4	<u>L18</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	(microcontroller or dsp) same l1	40	<u>L17</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	bus and l14	73	<u>L16</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l3 and l14	0	<u>L15</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l4 same l2	136	<u>L14</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l4 and l2	213	<u>L13</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l1 same l2	265	<u>L12</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l1 with l3	6	<u>L11</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	(l1 same l3) same l2	3	<u>L10</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	(l1 with l3) same l2	0	<u>L9</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l6 same l3	2	<u>L8</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l5 same l3	10	<u>L7</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	((processing unit) or microprocessor) same l1	208	<u>L6</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	(host or cpu) same l1	286	<u>L5</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l1 adj cell	872	<u>L4</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	system bus	24202	<u>L3</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	pla or pld or pga or fpla or fpld or fpga	19512	<u>L2</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	configuration adj (memory or buffer or storage)	5484	<u>L1</u>

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USPT,PGPB,JPAB,EPAB,DWPI,TDBD	15 and (17 or 18 or 19)	45	<u>L10</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	((716/16)!.CCLS.))	173	<u>L9</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	((326/41)!.CCLS.))	762	<u>L8</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	((326/39)!.CCLS.)	811	<u>L7</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	(system adj bus) same l4	3	<u>L6</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	bus same l4	82	<u>L5</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l1 same l2	267	<u>L4</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	l1 adj cell	872	<u>L3</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	pla or pld or fpla or fpld or pga or fpga	19512	<u>L2</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	configuration: adj (memory or library or buffer or storage)	5586	<u>L1</u>

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USPT,PGPB,JPAB,EPAB,DWPI,TDBD	17 and 16	35	<u>L9</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	((716/16)!.CCLS.) and 16	35	<u>L8</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	system adj bus	24202	<u>L7</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	(configuring or configure or configured) with 11	303	<u>L6</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	13 same 11	3	<u>L5</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	dma or dmac or (direct memory access\$3)	27964	<u>L4</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	pio or (programmable adj ((input adj outputs) or (i/o) or (inputs/outputs)))	2162	<u>L3</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	((716/16)!.CCLS.) and 11	68	<u>L2</u>
USPT,PGPB,JPAB,EPAB,DWPI,TDBD	configuration adj (memory or logic)	4262	<u>L1</u>